CDX-828

SERVICE MANUAL

US Model
Canadian Model
AEP Model
UK Model
E Model

Model Name Using Similar Mechanism	CDX-805
CD Drive Mechanism Type	MG-250C-137
Optical Pick-up Name	KSS-521A/J2N

SPECIFICATIONS

System: Compact disc digital audio system

Laser diode properties
- Material: GaAlAs
- Wavelength: 780 nm
- Emission Duration: Continuous
- Laser Output Power: Less than 44.6 µW*

* *This output is the value measured at a distance of 200 mm from the objective lens surface on the Optical Pick-up Block.*

Frequency response: 5 – 20,000 Hz

Wow and flutter: Below the measurable limit

Signal-to-noise ratio: 99 dB

Outputs:
- Optical digital output
- BUS control output (8 PIN)
- Analog audio output (RCA PIN)

Current drain:
- 800 mA (during CD playback)
- 800 mA (during loading or ejecting a disc)

Operating temperature: –10°C to +55°C (14°F to 131°F)

Dimensions: Approx. 262 × 90 × 181.5 mm ($10^3/_8 \times 3^5/_8 \times 7^1/_4$ in.) (w/h/d) not incl. projecting parts and controls

Mass: Approx. 2.1 kg (4 lb. 10 oz.)

Power requirement: 12 V DC car battery (negative ground)

Supplied accessories:
- Disc magazine (1)
- Parts for installation and connections (1 set)

Design and specifications subject to change without notice.

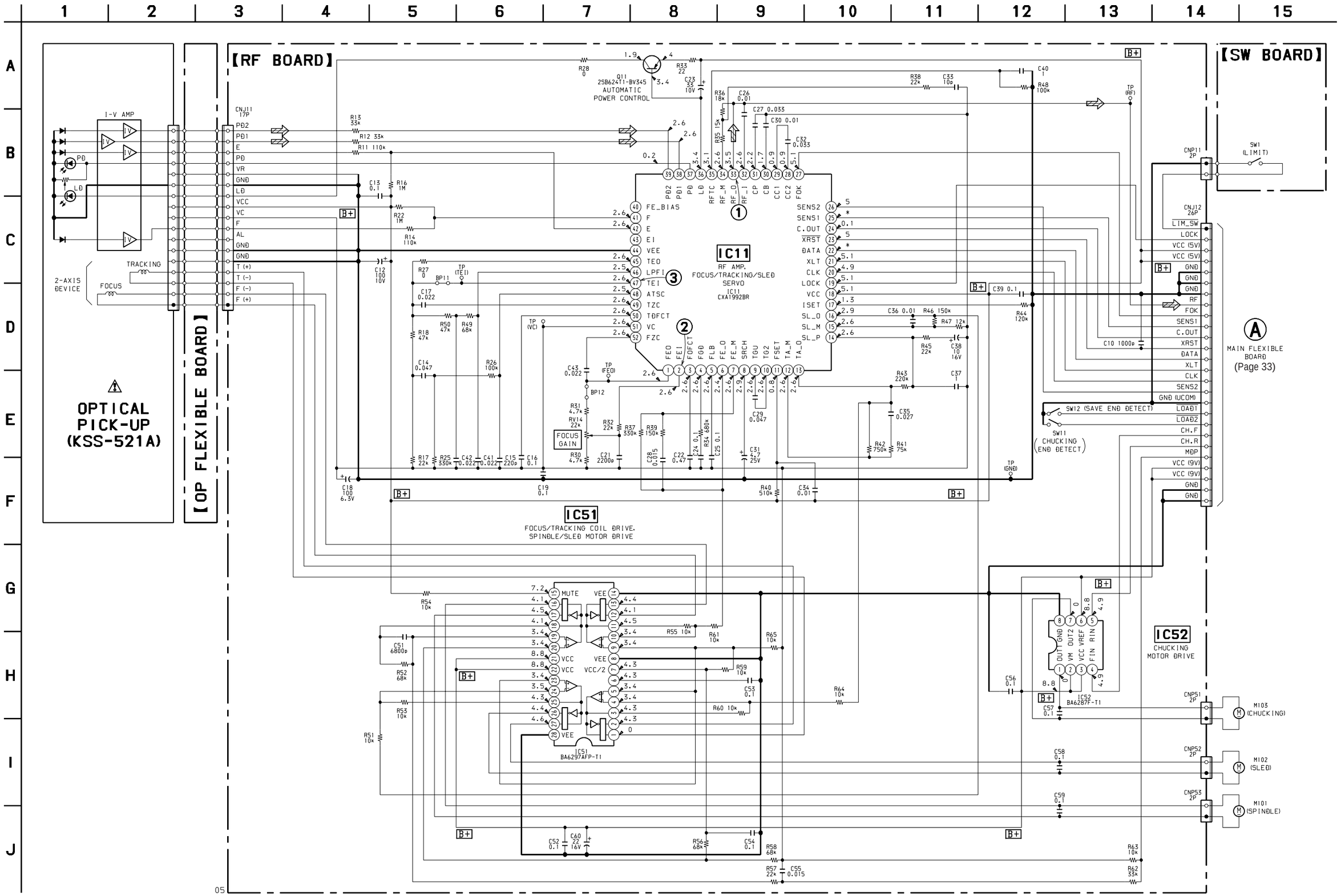
COMPACT DISC CHANGER

MICROFILM

SONY®

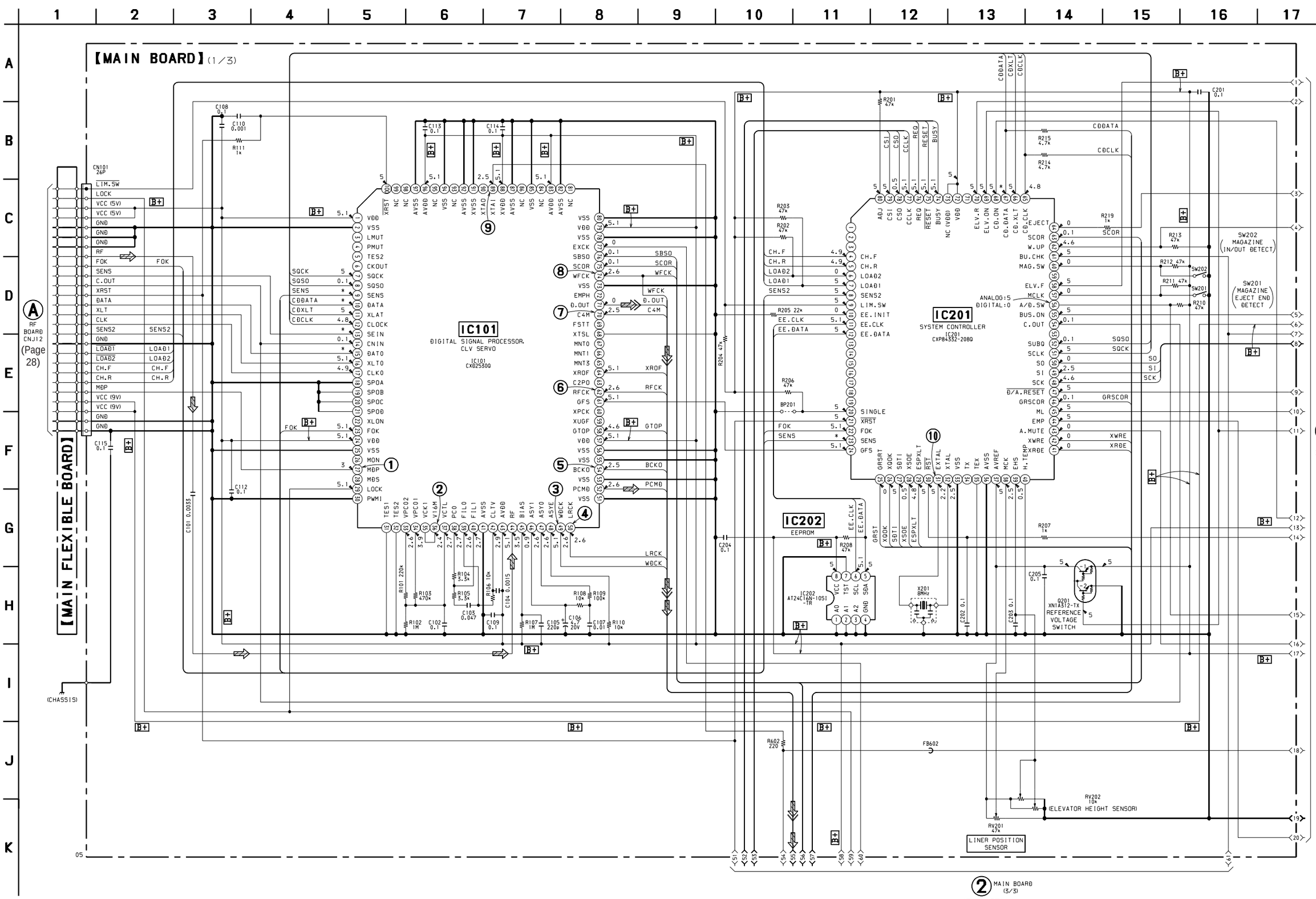
7-6. SCHEMATIC DIAGRAM – RF/SW Boards –

• See page 39 for Waveforms. • See page 45 for IC Block Diagrams.



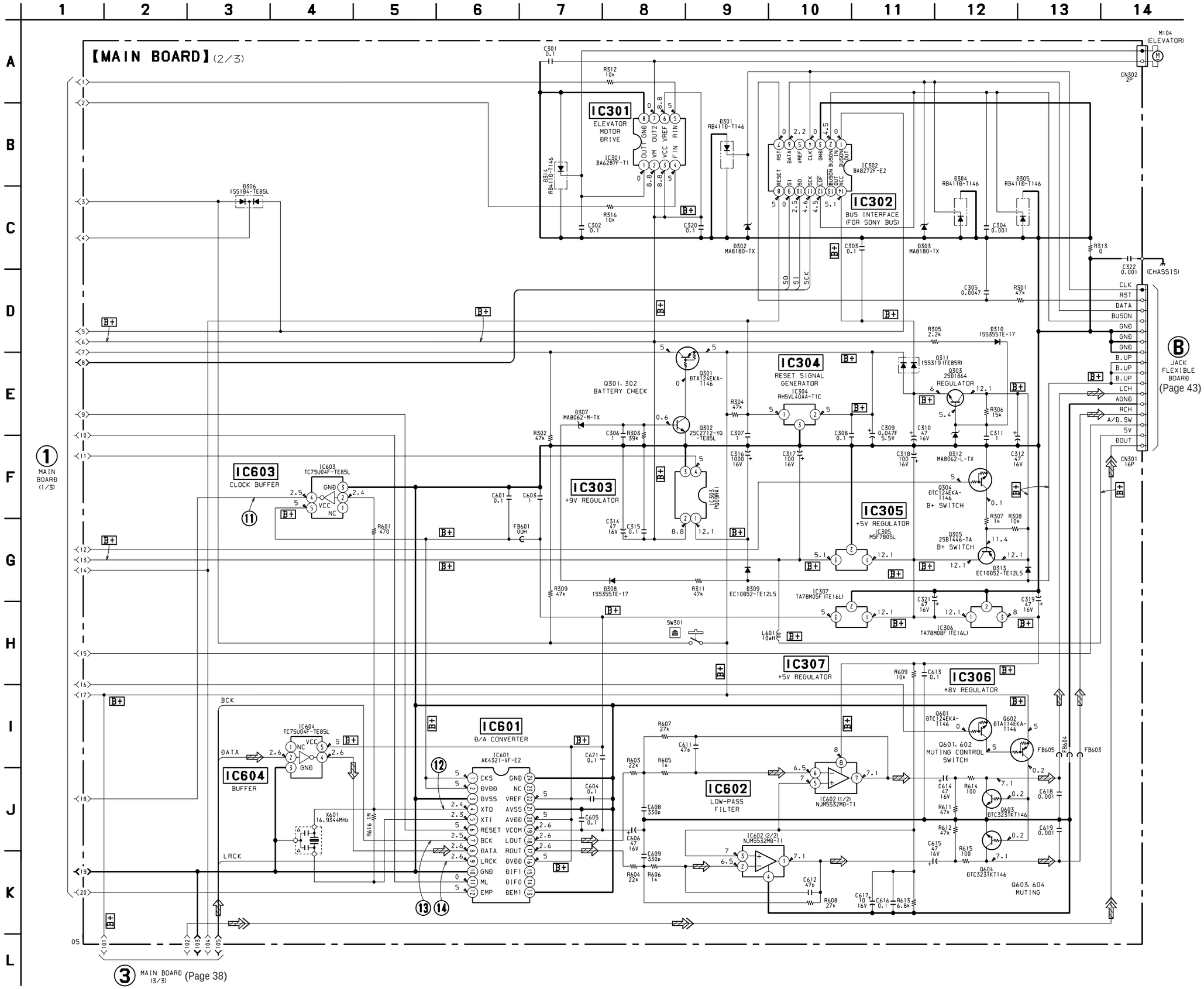
The components identified by mark ⚠ or dotted line with mark ⚠ are critical for safety. Replace only with part number specified.	Les composants identifiés par une marque ⚠ sont critiques pour la sécurité. Ne les remplacer que par une piéce portant le numéro spécifié.

7-9. SCHEMATIC DIAGRAM – MAIN Board (1/3) – • See page 39 for Waveforms. • See page 46 for IC Block Diagrams.



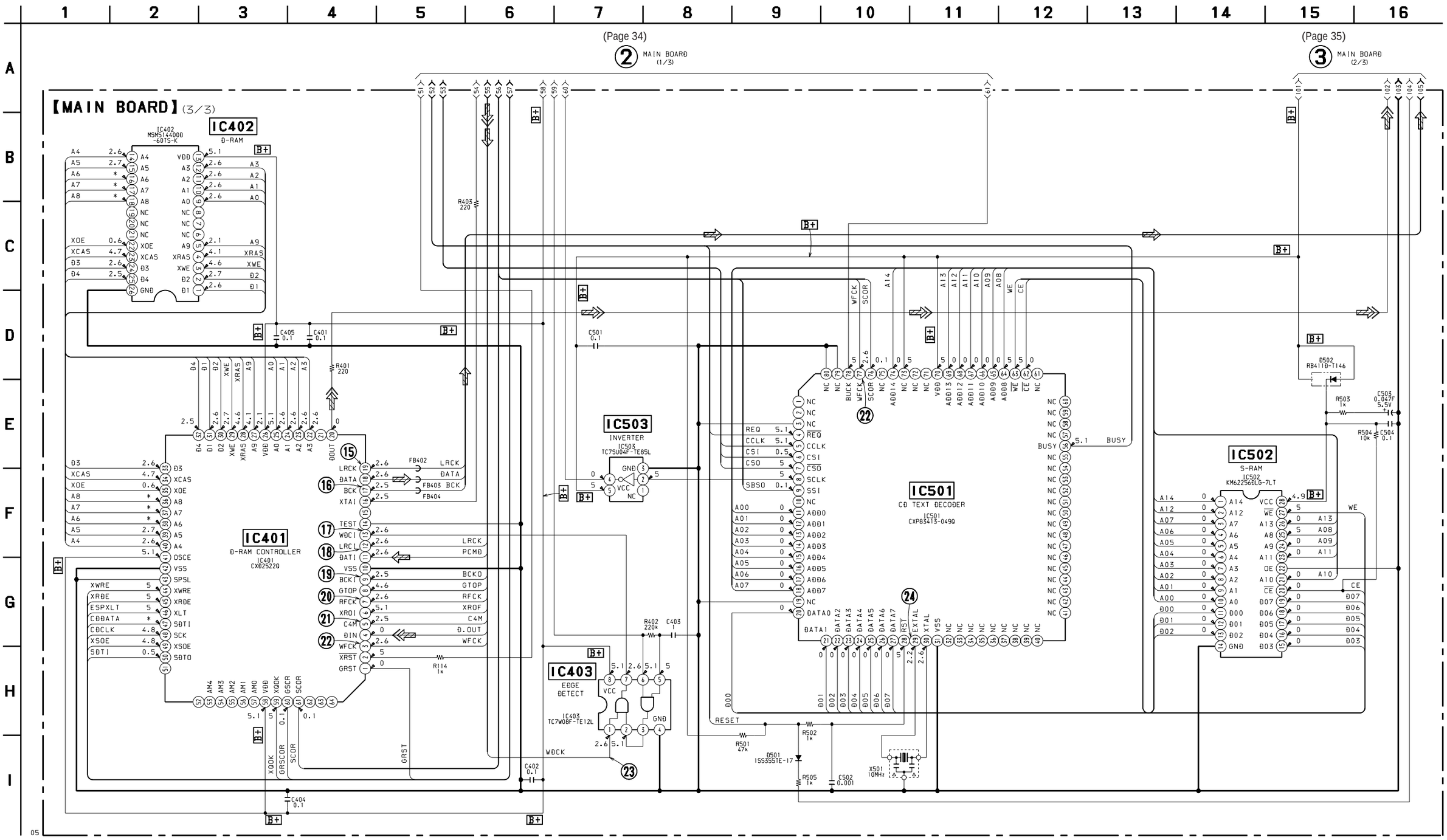
7-10. SCHEMATIC DIAGRAM – MAIN Board (2/3) –

• See page 40 for Waveforms. • See page 47 for IC Block Diagrams.



7-11. SCHEMATIC DIAGRAM – MAIN Board (3/3) –

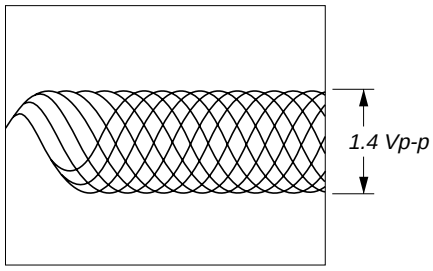
• See page 40 for Waveforms. • See page 47 for IC Block Diagrams.



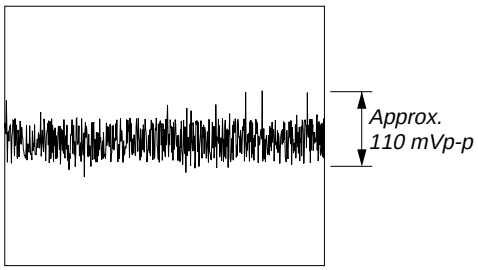
• **Waveforms**

– RF Board –

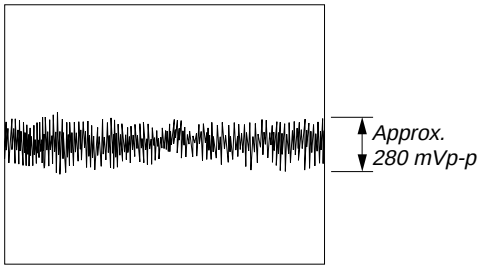
❶ IC11 ㉝ (RF O)
500 mV/DIV, 500 ns/DIV



❷ IC11 ② (FEI)
50 mV/DIV, 1 µs/DIV

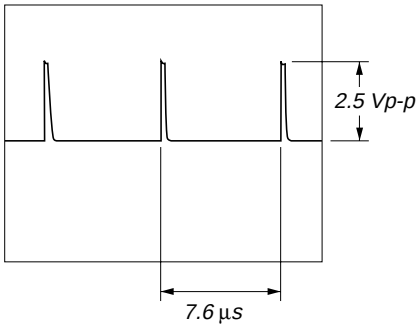


❸ IC11 ㊼ (TEI)
200 mV/DIV, 500 µs/DIV

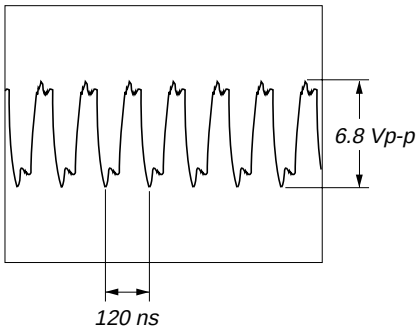


– MAIN Board (1/3) –

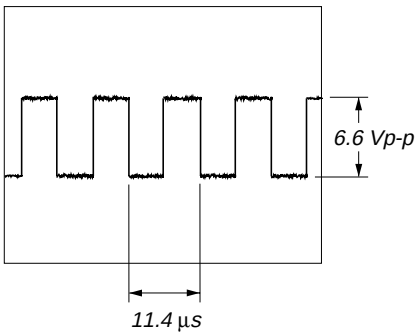
❶ IC101 ㉗ (MDP)



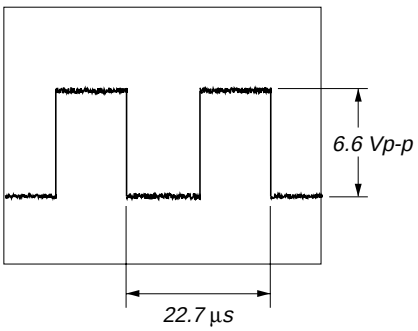
❷ IC101 ㊱ (V16M)



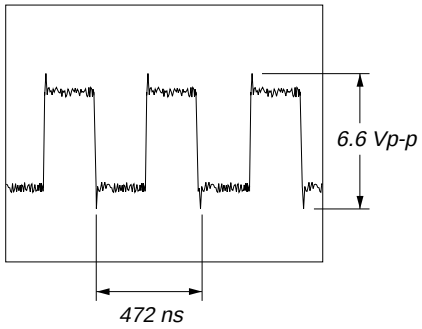
❸ IC101 ㊾ (WDCK)



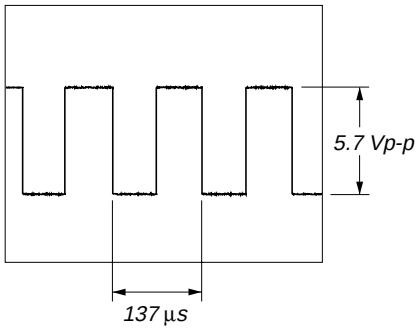
❹ IC101 ㊿ (LRCK)



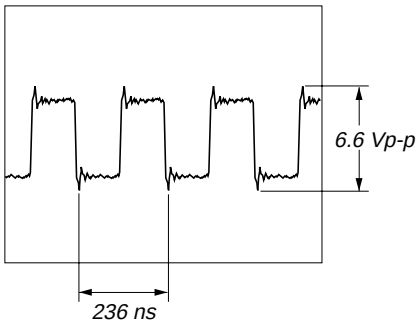
❺ IC101 ㊹ (BCKO)



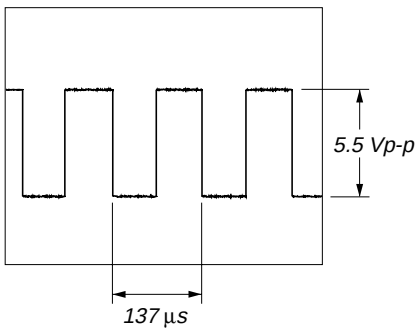
❻ IC101 ㊷ (RFCK)



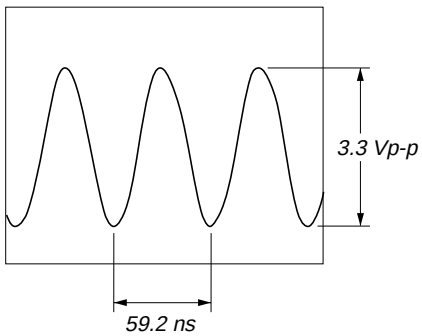
❼ IC101 ㊿ (C4M)



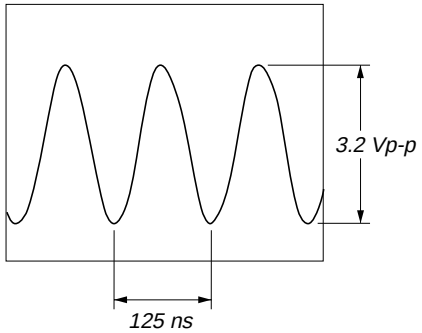
❽ IC101 ㊹ (WFCK)



❾ IC101 ㊾ (XTAI)

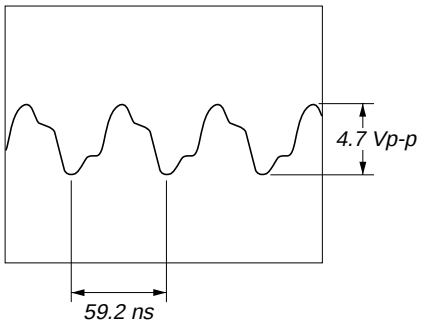


❿ IC201 ㉛ (EXTAL)

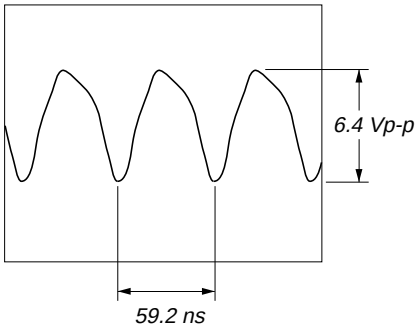


– MAIN Board (2/3) –

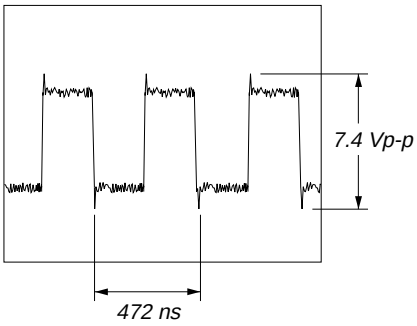
⓫ IC603 ④



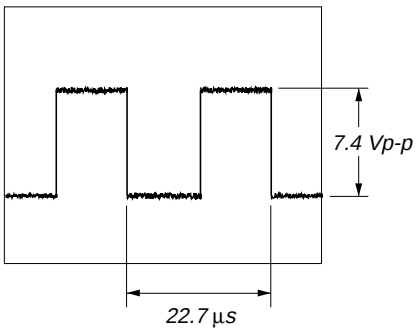
⓬ IC601 ④ (XTO)



⓭ IC601 ⑦ (BCK)

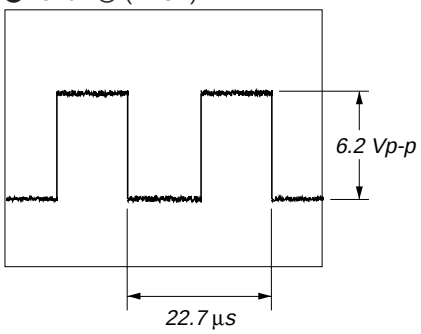


⓮ IC601 ⑨ (LRCK)

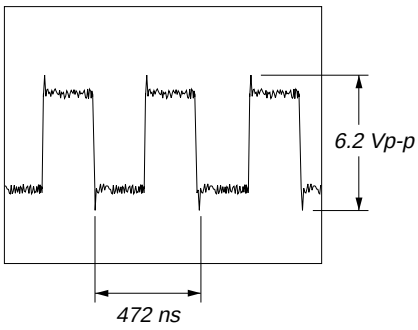


– MAIN Board (3/3) –

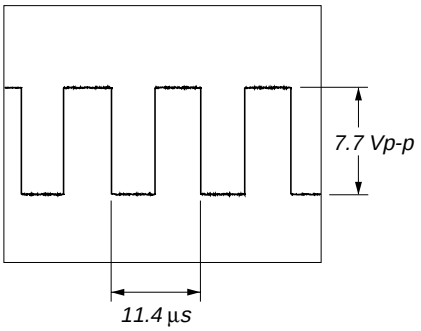
⓯ IC401 ⑲ (LRCK)



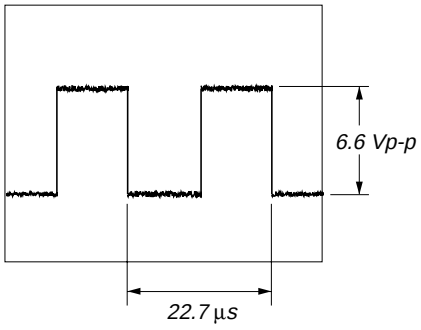
⓰ IC401 ⑰ (BCK)



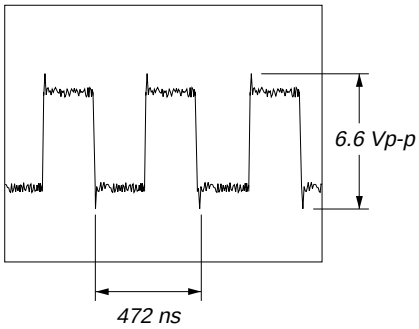
⓱ IC401 ⑬ (WDCI)



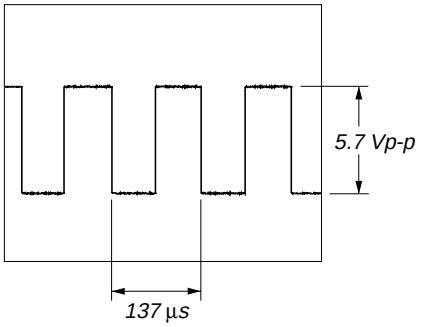
⓲ IC401 ⑫ (LRCI)



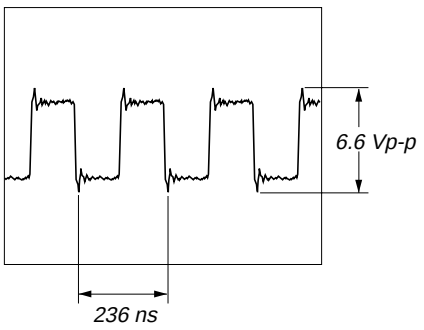
⓳ IC401 ⑨ (BCKI)



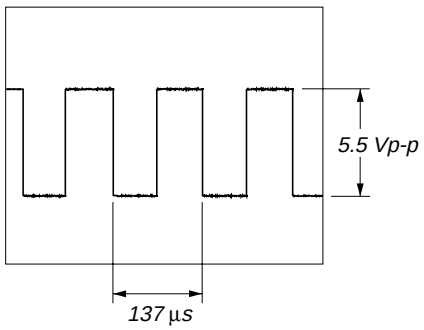
⓴ IC401 ⑦ (RFCK)



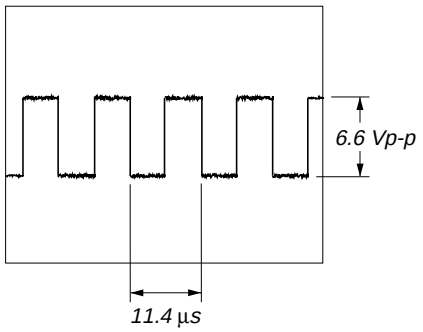
㉑ IC401 ⑤ (C4M)



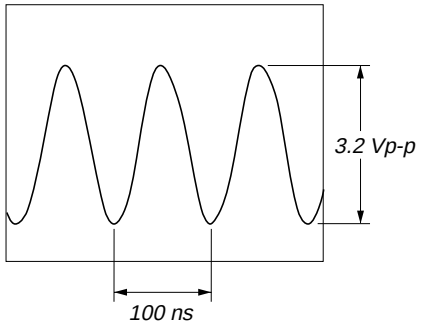
㉒ IC401 ③, IC501⑰ (WFCK)



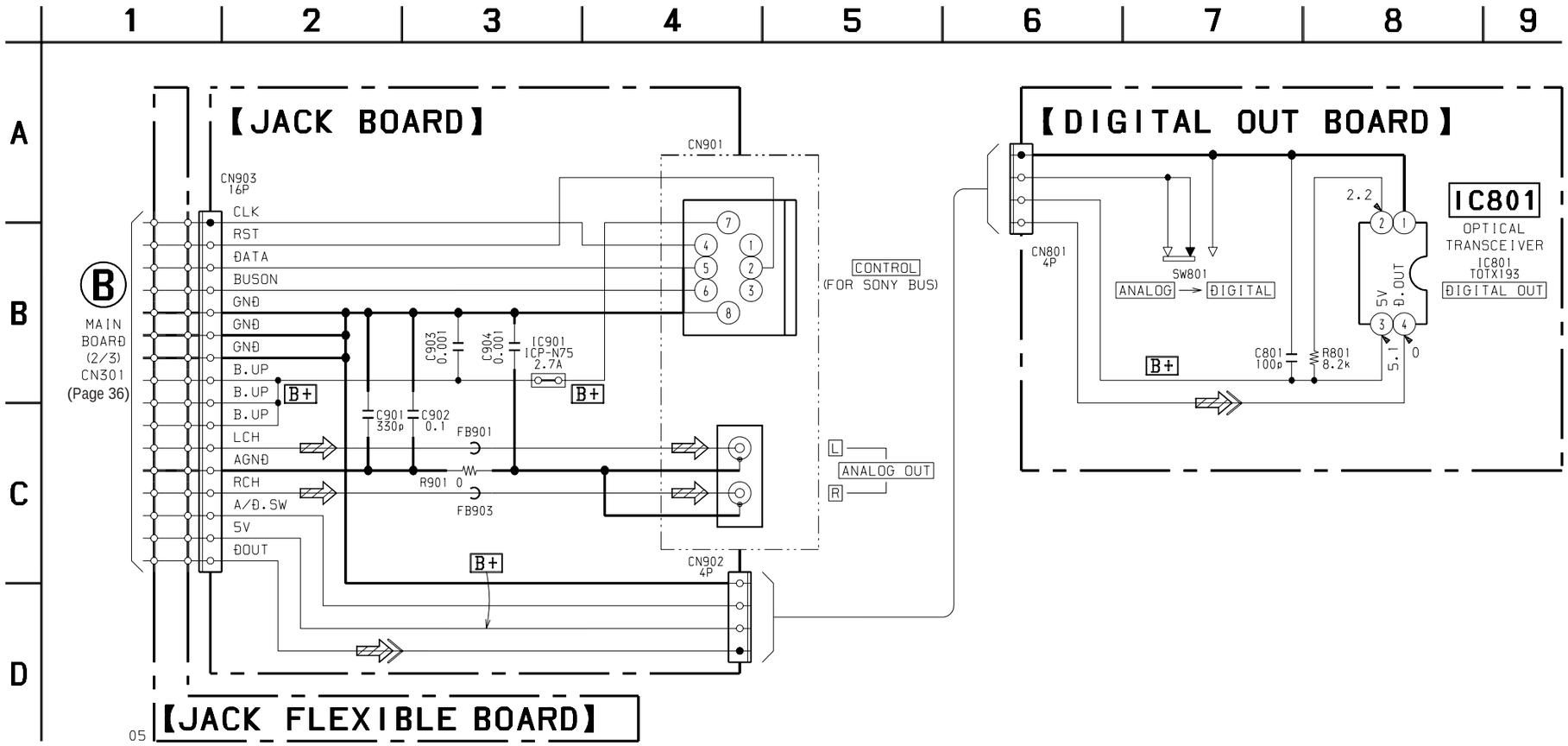
㉓ IC403 ①



㉔ IC501 ㉙ (EXTAL)

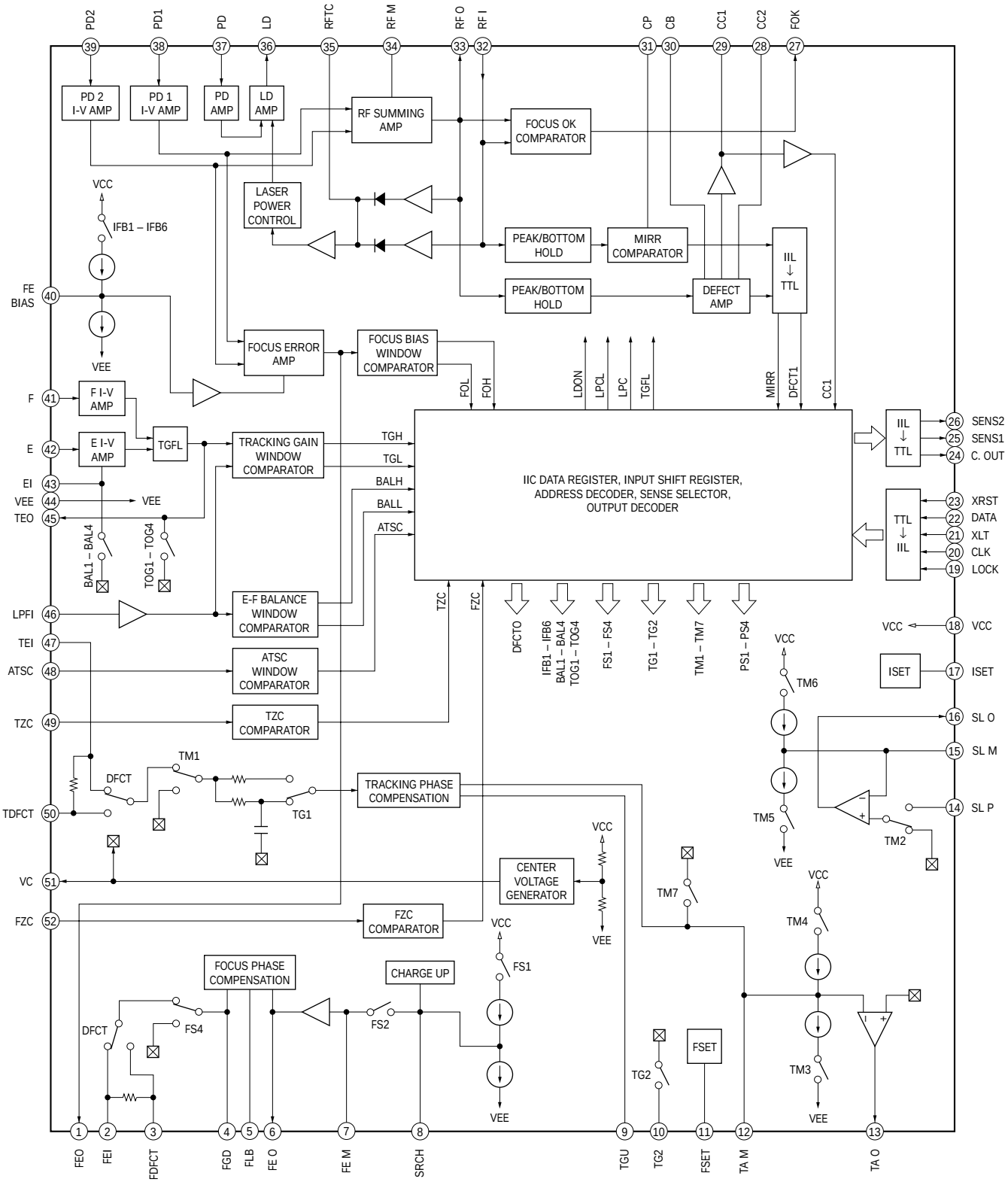


7-13. SCHEMATIC DIAGRAM – DIGITAL OUT/JACK Boards –

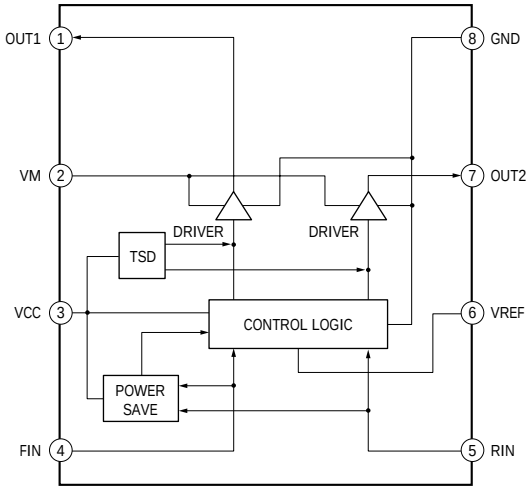


• **IC Block Diagrams**
– RF Board –

IC11 CXA1992BR

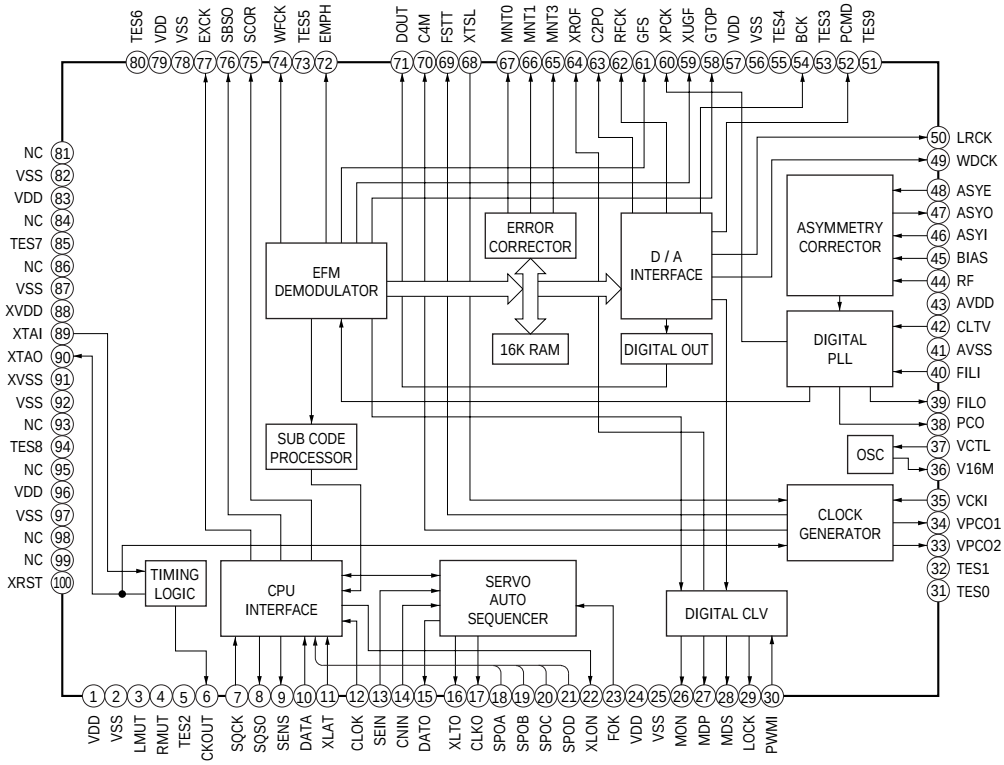


IC52 BA6287F

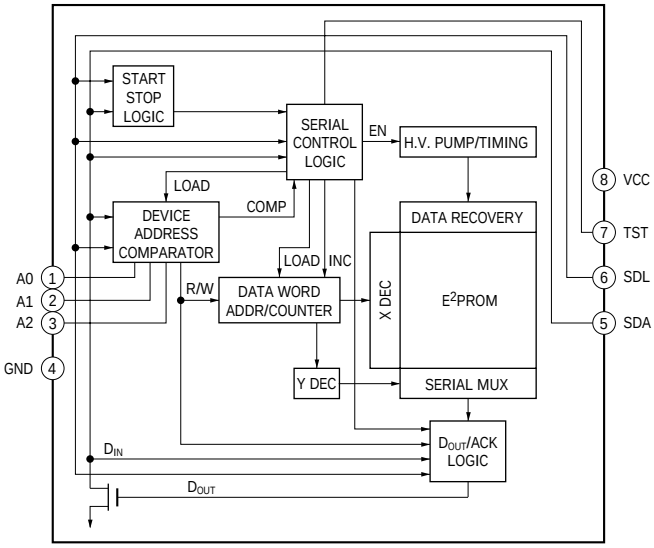


– MAIN Board –

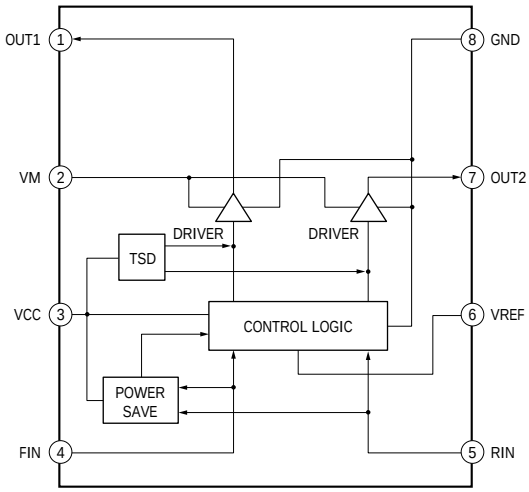
IC101 CXD2530Q



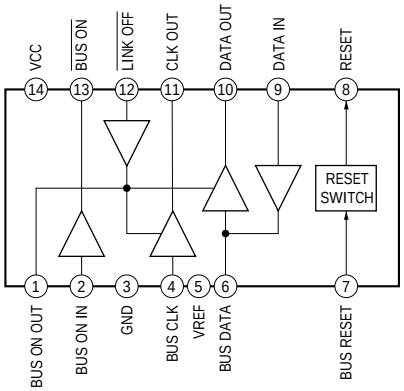
IC202 AT24C16N-10SI-TR



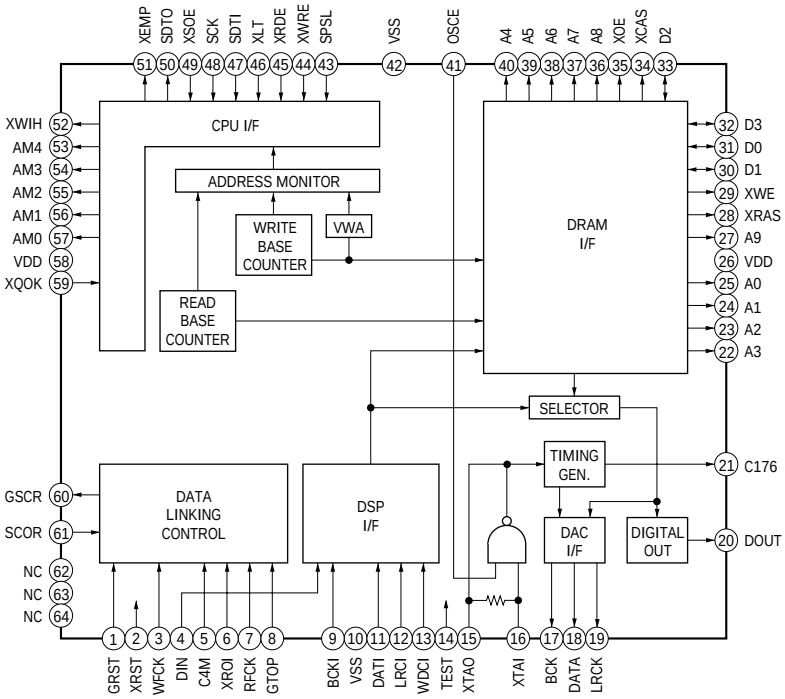
IC301 BA6287F



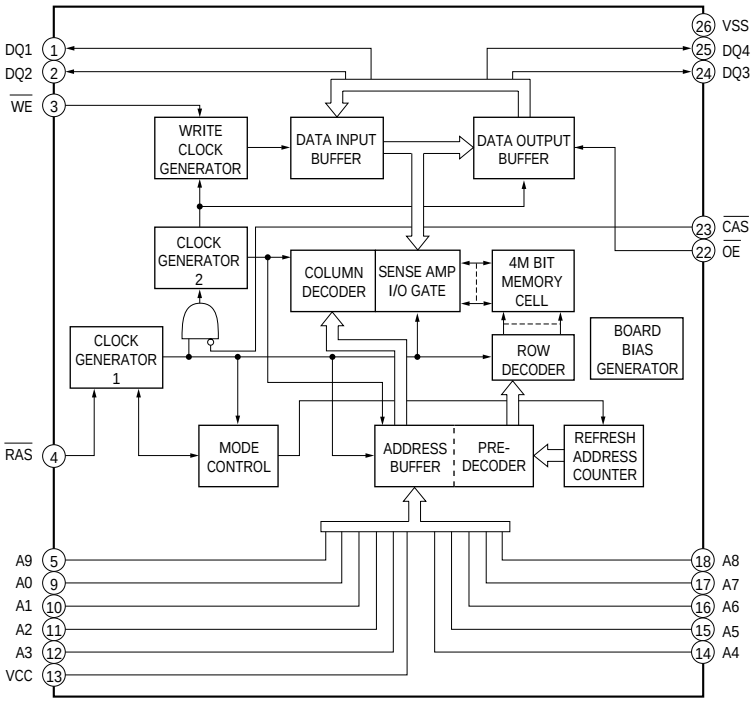
IC302 BA8272F-E2



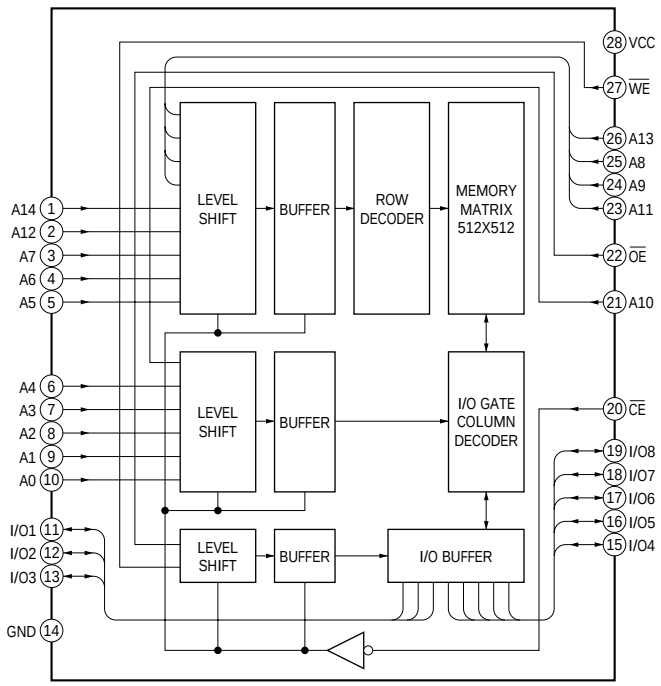
IC401 CXD2522Q



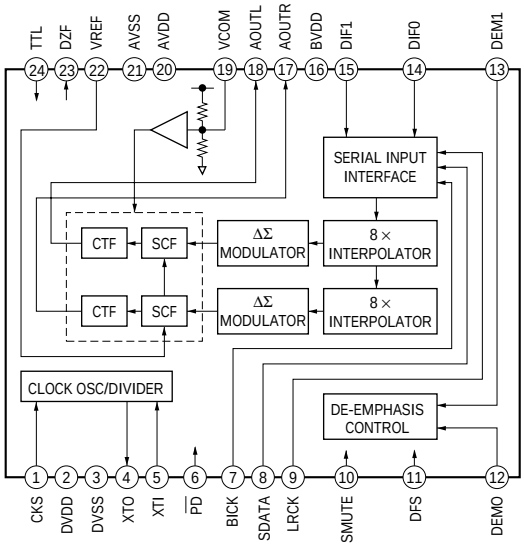
IC402 MSM514400D-60TS-K



IC502 KM62256DLG-7LT



IC601 AK4321-VF-E2



7-14. IC PIN FUNCTION DESCRIPTION

• MAIN BOARD IC201 CXP84332-208Q (SYSTEM CONTROLLER)

Pin No.	Pin Name	I/O	Function
1 to 3	—	O	Not used (open)
4	CH.F	O	Motor drive signal (load chucking direction) output to the chucking motor drive (IC52) "L" active *1
5	CH.R	O	Motor drive signal (save direction) output to the chucking motor drive (IC52) "L" active *1
6	LOAD2	I	Chucking end detect switch (SW11) input terminal "L": When completion of the disc chucking operation
7	LOAD1	I	Save end detect switch (SW12) input terminal "L": When completion of the disc chucking operation
8	SENS2	I	Internal status signal (sense signal) input from the CXA1992BR (IC11)
9	LIM.SW	I	Sled limit in detect switch (SW1) input terminal "L": When the optical pick-up is inner position
10	EE.INIT	I	Initialize signal input for the EEPROM (IC202) "H": format Fixed at "L" in this set
11	EE.CLK	O	Serial data transfer clock signal output to the EEPROM (IC202)
12	EE.DATA	I/O	Two-way data bus with the EEPROM (IC202)
13 to 19	—	O	Not used (open)
20	SINGLE	I	Setting terminal for the single disc/multiple discs mode "L": single mode, "H": multiple discs mode (fixed at "H")
21	$\overline{\text{XRST}}$	O	System reset signal output to the CXA1992BR (IC11), CXD2530Q (IC101) and CXD2522Q (IC401) "L": reset
22	FOK	I	Focus OK signal input from the CXA1992BR (IC11) "L": NG, "H": OK
23	SENS	I	Internal status signal (sense signal) input from the CXD2530Q (IC101)
24	GFS	I	Guard frame sync signal input from the CXD2530Q (IC101) "L": NG, "H": OK
25	GRSRT	O	Reset signal output to the CXD2522Q (IC401) "L": reset
26	XQOK	O	Subcode Q OK pulse signal output to the CXD2522Q (IC401) "L" active
27	SDTI	I	ESP status signal input from the CXD2522Q (IC401)
28	XSOE	O	ESP status read enable signal output to the CXD2522Q (IC401) "L" active
29	ESPXLT	O	ESP latch pulse signal output to the CXD2522Q (IC401) "L" active
30	$\overline{\text{RST}}$	I	System reset signal input from the SONY bus interface (IC302) and reset signal generator (IC304) "L": reset For several hundreds msec. after the power supply rises, "L" is input, then it changes to "H"
31	EXTAL	I	Main system clock input terminal (8 MHz)
32	XTAL	O	Main system clock output terminal (8 MHz)
33	VSS	—	Ground terminal
34	TX	O	Sub system clock output terminal Not used (open)
35	TEX	I	Sub system clock input terminal Not used (fixed at "L")
36	AVSS	—	Ground terminal (for A/D converter)
37	AVREF	I	Reference voltage (+5V) input terminal (for A/D converter)
38	MCK	I	Input of signal for the fine adjustment (linear position sensor adjustment; RV201) of elevator position (A/D input)
39	EHS	I	Elevator height position detect input from the RV202 (elevator height sensor) (A/D input)
40	H.TEMP	I	High temperature sensor input terminal Not used (fixed at "L")
41	XRDE	O	D-RAM read enable signal output to the CXD2522Q (IC401) "L" active
42	XWRE	O	D-RAM write enable signal output to the CXD2522Q (IC401) "L" active
43	A.MUTE	O	Audio line muting on/off control signal output terminal "H": muting on
44	EMP	O	Emphasis mode output to the D/A converter (IC601) "H": emphasis on
45	ML	O	Fast speed dubbing control signal output to the D/A converter (IC601) "L": fast speed
46	GRSCOR	I	Subcode sync (S0+S1) detection signal input from the CXD2522Q (IC401)

Pin No.	Pin Name	I/O	Function
47	$\overline{\text{D/A.RESET}}$	O	Reset signal output to the D/A converter (IC601) "L": reset
48	SCK	I	Serial data transfer clock signal input from the SONY bus interface (IC302)
49	SI	I	Serial data input from the SONY bus interface (IC302)
50	SO	O	Serial data output to the SONY bus interface (IC302)
51	SCLK	O	Subcode Q data reading clock signal output to the CXD2530Q (IC101)
52	SUBQ	I	Subcode Q data input from the CXD2530Q (IC101)
53	—	O	Not used (open)
54	C.OUT	I	Track number count signal input from the CXA1992BR (IC11)
55	BUS.ON	I	Bus on/off control signal input from the SONY bus interface (IC302) "H": bus on
56	A/D.SW	I	Analog/digital select switch (SW801) input terminal "L": digital, "H": analog
57	MGLK	I	Magazine eject operation completion detect switch (SW201) input "L": eject completed
58	ELV.F	O	Motor drive signal (elevator up direction) output to the elevator motor drive (IC301) "L" active *2
59	—	O	Not used (open)
60	MAG.SW	I	Magazine in/out detect switch (SW202) input "L": magazine detected
61	BU.CHK	I	Battery detection signal input terminal "H": battery on
62	W.UP	I	Bus on or eject switch (SW301) input terminal "H": bus on or eject switch pushing
63	SCOR	I	Subcode sync (S0+S1) detection signal input from the CXD2530Q (IC101)
64	EJECT	I	Eject switch (SW301) input terminal "H" active
65	CD.CLK	O	Serial data transfer clock signal output to the CXD2530Q (IC101) and CXD2522Q (IC401)
66	CD.XLT	O	Serial data latch pulse signal output to the CXD2530Q (IC101)
67	CD.DATA	O	Serial data output to the CXD2530Q (IC101) and CXD2522Q (IC401)
68	CD.ON	O	D/A converter and servo section power supply on/off control signal output "H": power on
69	ELV.ON	O	Mechanism deck section power supply on/off control signal output "H": power on
70	ELV.R	O	Motor drive signal (elevator down direction) output to the elevator motor drive (IC301) "L" active *2
71	—	O	Not used (open)
72	VDD	—	Power supply terminal (+5V)
73	NC (VDD)	—	Connected to the power supply (+5V)
74	BUSY	I	Busy monitor input from the CD text decoder (IC501) "L": busy status
75	$\overline{\text{RESET}}$	O	Reset signal output to the CD text decoder (IC501) "L": reset
76	REQ	I	Data request signal input from the CD text decoder (IC501) "L" active
77	CCCLK	O	Command clock signal output to the CD text decoder (IC501)
78	CSO	O	Command data output to the CD text decoder (IC501)
79	CSI	I	Command data input from the CD text decoder (IC501)
80	ADJ	I	Automatic/manual adjustment selection terminal "L": manual adjustment mode, "H": automatic adjustment mode (fixed at "H" in this set)

*1 chucking motor (M103) control

Mode / Terminal	STOP	LOAD CHUCKING	SAVE	BRAKE
CH.F (pin ④)	"H"	"L"	"H"	"L"
CH.R (pin ⑤)	"H"	"H"	"L"	"L"

*2 elevator motor (M104) control

Mode / Terminal	STOP	ELEVATOR UP	ELEVATOR DOWN	BRAKE
ELV.F (pin ㊽)	"H"	"L"	"H"	"L"
ELV.R (pin ㊿)	"H"	"H"	"L"	"L"

• **MAIN BOARD IC501 CXP83413-049Q (CD TEXT DECODER)**

Pin No.	Pin Name	I/O	Function
1, 2	NC	O	Not used (open)
3	NC	I	Not used (fixed at "L")
4	$\overline{\text{REQ}}$	O	Request signal output to the system controller (IC201) "L" active
5	CCLK	I	Serial data transfer clock signal input from the system controller (IC201)
6	CSI	I	Serial data input from the system controller (IC201)
7	$\overline{\text{CSO}}$	O	Serial data output to the system controller (IC201)
8	SCLK	O	Clock signal output for subcode data reading to the CXD2530Q (IC101)
9	SSI	I	Subcode data input from the CXD2530Q (IC101)
10	NC	O	Not used (open)
11 to 18	ADD0 to ADD7	O	Address signal output to the S-RAM (IC502)
19	NC	I	Not used (fixed at "L")
20 to 27	DATA0 to DATA7	I/O	Two-way data bus with the S-RAM (IC502)
28	$\overline{\text{RST}}$	I	System reset signal input from the system controller (IC201), SONY bus interface (IC302) and reset signal generator (IC304) "L": reset For several hundreds msec. after the power supply rises, "L" is input, then it changes to "H"
29	EXTAL	I	System clock input terminal (10 MHz)
30	XTAL	O	System clock output terminal (10 MHz)
31	VSS	—	Ground terminal
32 to 55	NC	O	Not used (open)
56	BUSY	O	Busy signal output to the system controller (IC201) "L": busy status
57 to 61	NC	O	Not used (open)
62	$\overline{\text{CE}}$	O	Chip enable signal output to the S-RAM (IC502) "L" active
63	$\overline{\text{WE}}$	O	Data write enable signal output to the S-RAM (IC502) "L" active
64 to 69	ADD8 to ADD13	O	Address signal output to the S-RAM (IC502)
70	VDD	—	Power supply terminal (+5V)
71, 72	NC	O	Not used (open)
73	NC	I	Not used (fixed at "H")
74	ADD14	O	Address signal output to the S-RAM (IC502)
75	NC	O	Not used (open)
76	SCOR	I	Subcode sync (S0+S1) detection signal input from the CXD2530Q (IC101)
77	WFCK	I	Write frame clock (7.35 kHz) signal input from the CXD2530Q (IC101)
78	BUCK	I	Backup power supply detection signal input terminal (used also to reset standby)
79, 80	NC	I	Not used (fixed at "L")